IN THE CLAIMS:

1. (Original) A method for processing a first memory request issued by a requestor and directed to a location in a memory, the first memory request containing an address corresponding to the memory location, the method comprising the steps of:

(A) associating the first memory request with a request identifier;

(B) selecting a memory device containing the memory location corresponding to the address;

(C) issuing a second memory request without the request identifier to the memory device to access information stored at the location;

(D) receiving the information from the memory device; and

(E) associating the information with the request identifier.

2. (Original) The method of claim 1 wherein the first memory request further contains the request identifier.

3. (Original) The method of claim 1 wherein the step of associating the first memory request with a request identifier further comprises the step of:

generating the request identifier.

4. (Original) The method of claim 1 further comprising the steps of:

determining if the memory device is available; and

performing steps C through E if the memory device is available.

5. (Original) The method of claim 1 further comprising the step of:

saving the address value and the request identifier.

6. (Original) The method of claim 1 wherein the requestor is a processor.

7. (Original) An apparatus for processing a first memory request issued by a requestor and directed to a location in a memory, the first memory request containing an address corresponding to the memory location, the apparatus comprising:

means for associating the first memory request with a request identifier;

means for selecting a memory device containing the memory location corresponding to the address;

means for issuing a second memory request without the request identifier to the memory device to access information stored at the location;

means for receiving the information from the memory device; and

means for associating the information with the request identifier.

8. (Original) The apparatus of claim 7 wherein the first memory request contains:

the request identifier.

9. (Original) The apparatus of claim 7 further comprising:

means for determining if the memory device is available.

10. (Original) The apparatus of claim 7 further comprising:

means for saving the request identifier.

11. (Original) The apparatus of claim 10 wherein the request identifier is saved in an entry in a table.

12. (Original) The apparatus of claim 7 wherein the first memory request contains

a port of origin.

13. (Original) The apparatus of claim 7 wherein the requestor is a processor.

14. (Original) A circuit for processing a first memory request issued by a requestor and directed to a location in a memory, the memory comprising one or more memory devices, the first memory request containing an address corresponding to the memory location, the circuit comprising:

a system controller connected to the requestor and the memory, the system controller configured to receive the first memory request from the requestor, associate the first memory request with a request identifier and in response to the first memory request, select one or more memory devices and issue one or more second memory requests without the request identifier to each of the selected memory devices.

15. (Original) The apparatus of claim 14 wherein the system controller further comprises:

a table comprising one or more entries, each entry formatted with a request identifier field and an address field, the request identifier field holding the request identifier and the address field holding the address.

16. (Original) The circuit of claim 14 wherein the requestor is a processor.

17. (Original) An intermediate node configured to process a first memory request directed to a location in a memory, the memory comprising one or more memory devices, the first memory request containing an address corresponding to the memory location, the intermediate node comprising:

a requestor configured to issue the first memory request;

a system controller coupled to the requestor, the system controller configured to receive the first memory request, associate the first memory request with a request identifier and in response to the first memory request select one or more memory devices and issue one or more second memory requests without the request identifier to each of the selected memory devices; and

one or more memory devices coupled to the system controller, the memory devices configured to receive the one or more second memory requests and return information in response to the second memory requests.

18. (Original) The intermediate node of claim 17 wherein the system controller further comprises:

a table comprising one or more entries, each entry formatted with a request identifier field and an address field, the request identifier field holding the request identifier and the address field holding the address.

19. (Original) The intermediate node of claim 17 wherein the requestor is a processor.

20. (Original) A computer readable medium comprising computer executable instructions for performing method recited in claims 1, 3, 4 or 5.

21. (Previously Presented) Electromagnetic signals propagating on a computer network, comprising:

said electromagnetic signals carrying instructions for execution on a processor for the practice of the method recited in claims 1, 3, 4 or 5.